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AREA EFFICIENT DESIGN AND IMPLEMENTATION OF FM0/MANCHESTER ENCODING USING SOLS TECHNIQUE FOR DSRC APPLICATIONS

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***ABSTRACT*:**
The dedicated short-range communication (DSRC) is an emerging technique to push the intelligent transportation system into our daily life. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. In this paper, the similarity oriented logic simplification (SOLS) technique is proposed to overcome this limitation. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. The performance of this paper is evaluated on the post layout simulation in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm 1P6M CMOS technology. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98×30.43 μm2. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.

Keywords: Dedicated short-range communication (DSRC), FM0, Manchester, VLSI.

I. INTRODUCTION

Manchester coding technique is a digital coding technique in which all the bits of the binary data are arranged in a particular sequence. Here a bit '1' is represented by transmitting a high voltage for half duration of the input signal and for the next halftime period an inverted signal will be send. When transmitting '0' in Manchester format, for the first half cycle a low voltage will send, and for the next half cycle a high voltage is send. The advantage of Manchester coding is that, when sending a data having continuous high signals or continuous low signal (e.g.: 11110000), it is difficult to calculate the number of 1 S and Os in the data. Because there is no transition from low to high or high to low for a particular time period (Here it is 4 x T, T is the time duration for a single pulse). The detection is possible only by calculating the time duration of the signal. But when we code this signal in Manchester format there will always be a

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transition from high to low or low to high for each bit. Thus for a receiver it is easier to detect the data in Manchester format and also the probability for occurrence of an error is very low in Manchester format and it is a universally accepted digital encoding technique.

The dedicated short range communication is a protocol for one or two way medium range communication. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to roadside. In automobile to automobile, the DSRC enables the message sending and broadcasting among automobile. The automobile to roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC).

The DSRC architecture having the transceiver. The transceiver having the baseband processing, RF front end and microprocessor. The microprocessor is used to transfer the instruction to the baseband processing and RF front end. The RF front end is used to transmit and receive the wireless signals using the antenna.

The baseband processing is responsible for modulation, error correction, encoding and synchronization. The transmitted signal consists of the arbitrary binary sequence, it is very difficult to obtain the dc-balance.the fm0 and Manchester is providing the transmitted signal and then the dc-balance. The (SOLS) similarity oriented logic simplification having the two methods: area compact retiming and balance logic operation sharing. The area compact retiming used to reduce the transistor counts. The balance logic operation sharing is used to combine the fm0 and Manchester encoding.

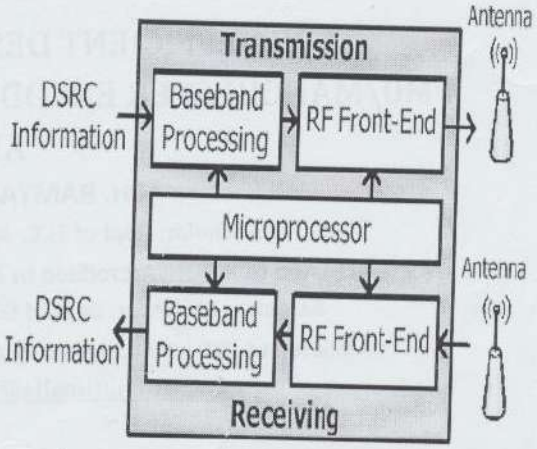

Fig. 1. System architecture of DSRC transceiver

The system architecture of DSRC transceiver is shown in Fig. 1. The upper and bottom parts are dedicated for transmission and receiving, respectively. This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through the antenna. The DSRC standards have been established by several organizations in different countries. These DSRC standards of America, Europe, and Japan are shown in Table I. The data rate individually targets at 500 kb/s, 4 Mb/s, and 27 Mb/s with carrier frequency of 5.8 and 5.9 GHz. The modulation methods incorporate amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the waveform of transmitted signal is expected to have zero mean for robustness issue, and this is also referred to as dc-balance.

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II. LITERATURE SURVEY

The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc-balance. The purposes of FM0 and Manchester codes can provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely adopted in encoding for downlink. The VLSI architectures of FM0 and Manchester encoders are reviewed as follows.

A. Review of VLSI Architectures for FM0 Encoder and Manchester Encoder:

The literature [4] proposes VLSI architecture of Manchester encoder for optical communications. This design adopts the CMOS inverter and the gated inverter as the switch to construct Manchester encoder. It is implemented by 0.35-μm CMOS technology and its operation frequency is 1 GHz. The literature [5] further replaces the architecture of switch in [4] by the nMOS device. It is realized in 90-nm CMOS technology, and the maximum operation frequency is as high as 5 GHz. The literature [6] develops a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) applications. This design is realized in 0.35-μm CMOS technology and the maximum operation frequency is 200 MHz. The literature [7] also proposes a Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is conducted from the finite state machine (FSM) of Manchester code, and is realized into field-programmable gate array (FPGA) prototyping system. The maximum operation frequency of this design is about 256 MHz. The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator [8]. Its maximum operation frequency is about 192 MHz. Furthermore, [9] combines frequency shift keying (FSK) modulation and demodulation with Manchester codec in hardware realization.

III. CODING PRINCIPLES OF FM0 CODE AND MANCHESTER CODE

In the following discussion, the clock signal and the input data are abbreviated as CLK, and X, respectively. With the above parameters, the coding principles of FM0 and Manchester codes are discussed as follows.

FM0 Encoding As shown in Fig. 2, for each X, the FM0 code consists of two parts: one for former-half cycle of CLK, A, and the other one for later-half cycle of CLK, B. The coding principle of FM0 is listed as the following three rules.

1) If X is the logic-0, the FM0 code must exhibit a transition between A and B.

2) If X is the logic-1, no transition is allowed between A and B.

3) The transition is allocated among each FM0 code no matter what the X is.

An FM0 coding example, at cycle 1, the X is logic-0; therefore, a transition occurs on its FM0 code, according to rule 1. For simplicity, this transition is initially set from logic-0 to -1. According to rule 3, a transition is allocated among each FM0 code, and thereby the logic-1 is changed to logic-0 in the beginning of cycle 2. Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the X of logic-1. Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

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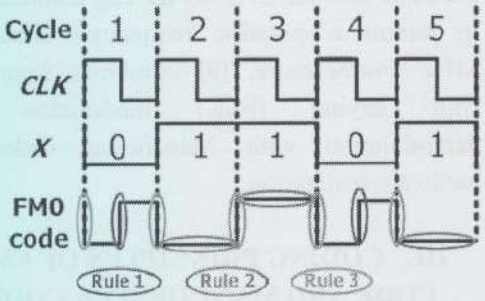

Fig. 2 Illustration of FM0 coding example

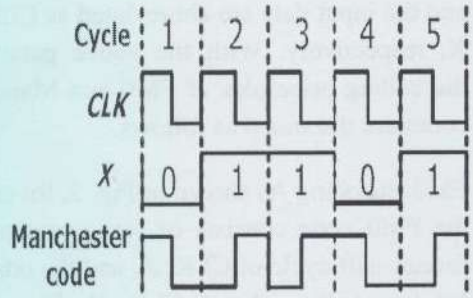

Fig. 3 Illustration of Manchester coding

Hardware Architecture of Fm0/Manchester Code:

This is the hardware architecture of the fm0/Manchester code. the top part is denoted the fm0 code and then the bottom part is denoted as the Manchester code. In fm0 code the DFFA and DFFB are used to store the state code of the fm0 code and also mux_1 and not gate is used in the fm0 code. When the mode=0 is for the fm0 code. The Manchester code is developed only using the XOR gate and when the mode=1 is for the Manchester code. The hardware utilization rate is defined as the following:

$$HUR = \frac{Active\ components}{total\ components} \times 100$$

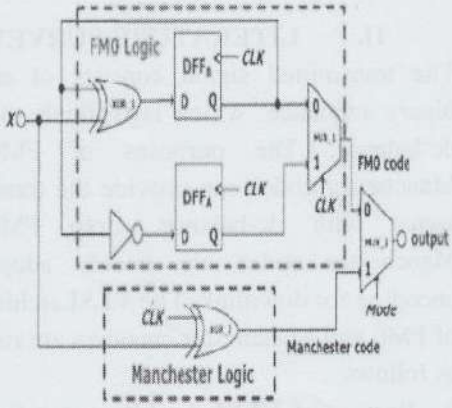

Fig. 4 Hardware architecture of Fm0/Manchester Code

The active components means the components are work in the both fm0 and Manchester code. The total components means the number of the components are present in the whole circuit. The HUR rate is given below the following section

TABLE

Coding	Active components(transistor count)/ total components (transistor count)	HUR
FM0	6(86)/7(98)	85.71%
MANCHESTER	2(26)/7(98)	28.57%
AVERAGE	4(56)/7(98)	57.14%

For both the encoding methods the total components is 7.for the fm0 code the total component is 7 and then the active component is 6.in Manchester code the total component is 7 the active component is 2.in both coding having 98 transistors are used without SOLS. The fm0 has 86 transistors, and then the Manchester having the 26 transistor. The average for both coding is 56 transistors

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.In proposed work reduces the total components from 7 to 6 and reduce the transistor counts. In this paper two multiplexer is used in proposed work reduce two multiplexer from one multiplexer, when reduce the multiplexer the total components are reduced the area and then the power consumption also reduced.

IV. FM0 AND MANCHESTER ENCODER USING SOLS TECHNIQUE:

The SOLS technique is classified into two parts area compact retiming and balance logic operation sharing.

A. Area compact retiming:

For fm0 the state code of the each state is stored into DFFA and DFFB .the transition of the state code is only depends on the previous state of B(t-1) instead of the both A(t-1) and B(t-1).

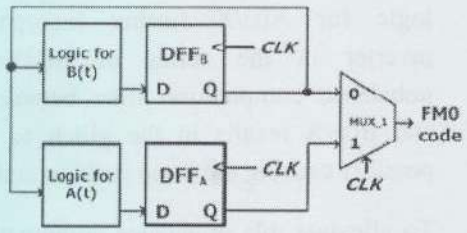

Fig. 5. FM0 encoding with Area compact retiming

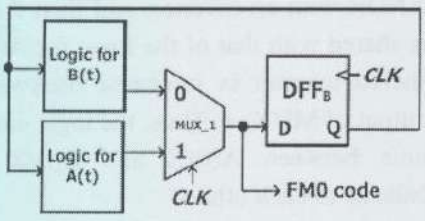

Fig. 6.FM0 encoding without area compact retiming

The previous state is denoted as the A(t-1) and then the B(t-1).and then the current state is denoted as the A(t) and then the B(t). Thus, the FM0 encoding just requires a single 1-bitflip-flop to store the previous value B(t−1).If the DFFA is directly removed, a non synchronization between A(t) and B(t)causes the logic fault of FM0 code. To avoid this logic-fault, the DFFB is relocated right after the MUX−1, where the DFFB is assumed is positive-edge triggered flip flop. At each cycle, the FM0 code, comprising A and B, is derived from the logic of A(t) and the logic of B(t), respectively. The FM0 code is alternatively switched between A(t) and B(t) through the MUX−1 by the control signal of the CLK. In the Q of DFFB is directly updated from the logic of B(t) with 1-cycle latency. When the CLK is logic-0, the B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. The timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. The B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. the timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. The transistor count of the FM0 encoding architecture without area-compact retiming is 72, and that with area-compact retiming is 50. The area-compact retiming technique reduces 22 transistors.

B. Balance logic operation sharing

The Manchester encoding is derived using the XOR operation. The equation of the XOR gate is given below.

$$X \oplus CLK = X\,CLK + \sim X\,CLK$$

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The concept of balance logic-operation sharing is to integrate the X into A(t) and X into B(t).the fm0 and Manchester logics have a common point of the multiplexer like logic with the selection of the CLK. the diagram for the balance logic operation sharing given the following. The A(t) can be derived from an inverter of B(t − 1), and X is obtained by an inverter of X. The logic for A(t)/X can share the same inverter, and then a multiplexer is placed before the inverter to switch he operands of B(t − 1) and X. The Mode indicates eitherFM0 or Manchester encoding is adopted. The similar concept can be also applied to the logic for B(t)/X

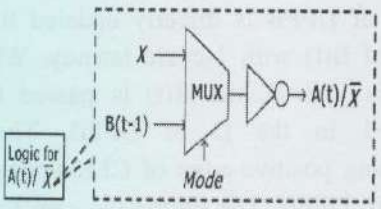
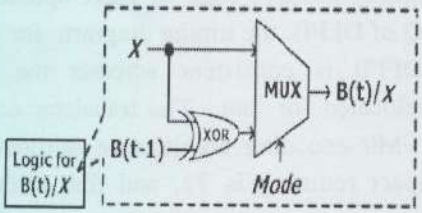


Fig. 7 Balance logic-operation sharing of A(t) and X.



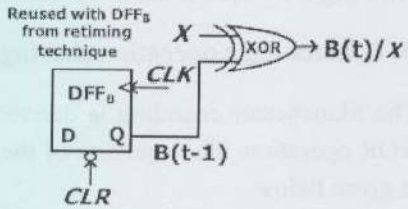


Fig.8. Balance logic-operation sharing of *B(t)* and *X*

Nevertheless, this architecture exhibits a drawback that the XOR is only dedicated for FM0 encoding, and is not shared with Manchester encoding. Therefore, the HUR of this architecture is certainly limited. The X can be also interpreted as the X 0, and thereby the XOR operation can be shared with Manchester and FM0 encodings, where the multiplexer irresponsible to switch the operands of B(t−1) and logic-0. This architecture shares the XOR for both B(t) and X, and there by increases the HUR. When the FM0 code is adopted, the CLR is disabled, and the B(t −1) can be derived from DFFB.

Hence, the multiplexer can be totally saved, and its function can be completely integrated into the relocated DFF. The logic for A(t)/X includes the MUX−2 and an inverter. Instead, the logic for B(t)/X just incorporates a XOR gate. In the logic for A(t)/X, the computation time of MUX−2 is almost identical to that of XOR in the logic for B(t)/X. However, the logic for A(t)/X further incorporates an inverter in the series of MUX−2. This unbalance computation time between A(t)/X and B(t)/X results in the glitch to MUX−1, possibly causing the logic fault on coding.

To alleviate this unbalance computation time, the architecture of the balance computation time between A(t)/X and B(t)/X. The XOR in the logic for B(t)/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for A(t)/X. This shared inverter is relocated backward to the output of MUX−1. Thus, the logic computation time between A(t)/X and B(t)/X is more balance to each other.

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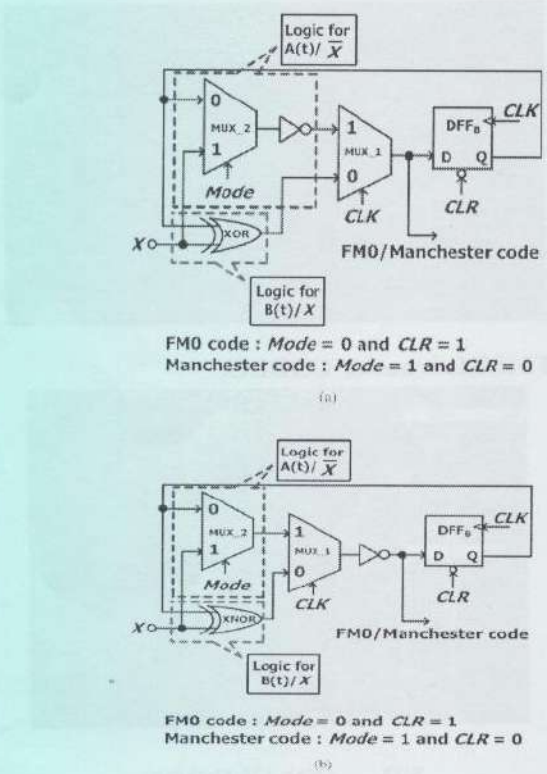


Fig. 9. VLSI architecture of FM0 and Manchester encodings using SOLS technique. (a) Unbalance computation time between A(t)/Xand B(t)/X. (b) Balance computation time

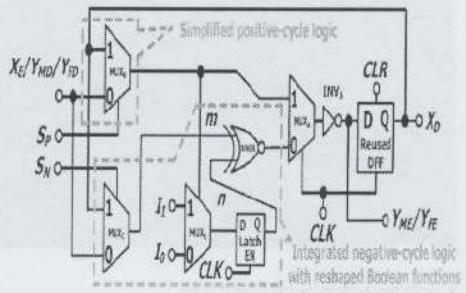
The adoption of FM0 or Manchester code depends on Mode and CLR. In addition, the CLR further has another individual function of a hardware initialization. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller. Whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved.

V. FM0/MANCHESTER CODEC

Dedicated short-range communication (DSRC) is a suitable method to realize infrastructures, vehicles, and sensor nodes. In DSRC, a wireless link is established between two basic units: on-board unit (OBU) and roadside unit (RSU). The OBU should be equipped with a DSRC transceiver to interact with RSU and the OBU activates either transmitting function or receiving function one at a time. They can be classified into two categories: full-cycle-based coding and half-cycle based coding. The full-cycle-based coding means the encoded symbol of a 1-bit data has a steady signal level within a cycle without any transition. The half-cycle-based coding means the encoded symbol of a 1-bit data allows a transition on signal level within a cycle, and both FM0 and Manchester belong to it.

Hence, this work proposes a half-cycle processing model (HCPM) to enable FM0/Manchester codec to be performed with efficient hardware utilization rate (HUR). The below figure performs encoding when (S_P,S_N,I_1,I_0) is 1001,0101 and performs decoding

When (S_P,S_N,I_1,I_0) is 0010,0011.



Proposed VLSI hardware architecture of FM0/Manchester codec

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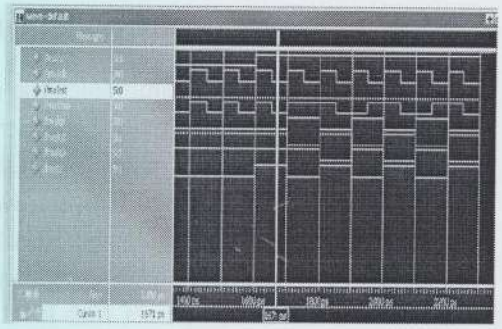
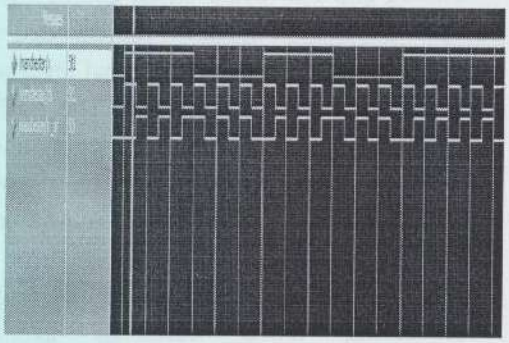
VI. SIMULATION RESULTS

FM0 Module:



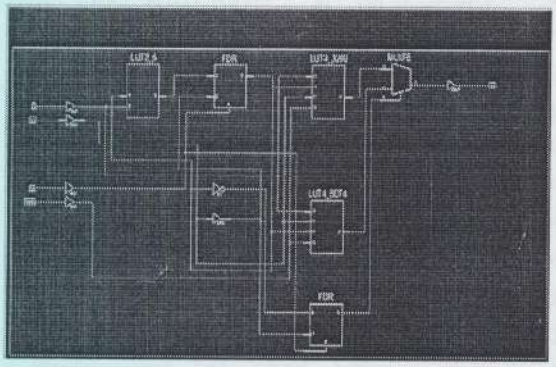
FM0 Code

Manchester:

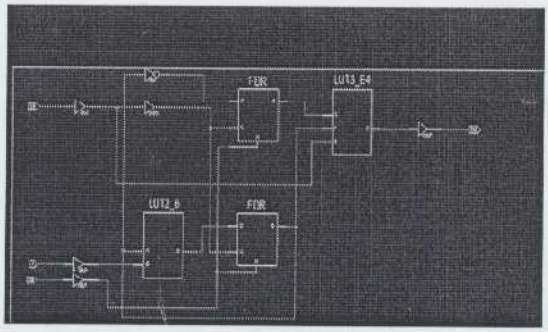


Manchester Coding

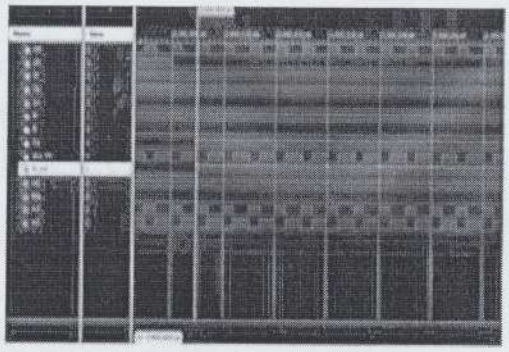
RTL Schematic:



Technology Schematic:



FM0/Manchester CODEC:



VII. CONCLUSION

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. The SOLS technique eliminates the limitation on hardware utilization by two core techniques area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding existing works.

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